Counter 0 to 59

Javier Mondragón Martin del Campo

Laboratory exercise number:

Lab. 7

Laboratory exercise name:

Assignment 7

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| Names: | Roll Number | Date |
| Javier Mondragón M. | A01365137 | 25/October/2019 |

Lab description:

The purpose of this laboratory is to learn how program a counter using clocks and two 7 segment displays on the Nexys.

The material used was:

Nexys 3 by Digilent for the FPGA

ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

Schematics, block diagrams and/or timing diagrams:

Using different VHDL codes, I formed different components and wire them on a TOP file and wire it. The components were not new, they are the same codes writed on previous classes. The following diagram shows how it works and the code displayed on the following images:

Frequency

Divider 1Hz

7-Seg Display

Unit selector

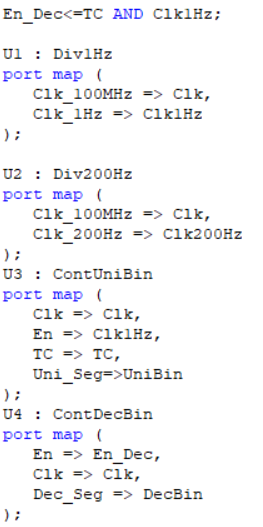
Counter

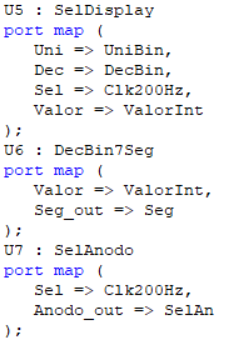
Anode Selector

Display Selector

Frequency Divider 200Hz

Code:





Results obtained:

The result was a successful counter from 0 to 59 seconds displayed on two segments.

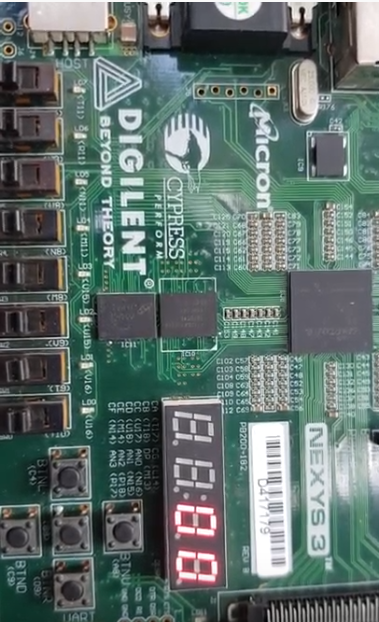
Evidence:

Video: https://youtu.be/kF23Jw3tEI0

Case 1: Case 2:

Case 3: Case 4:

Conclusions:

This way of programming in VHDL is more efficient and helps to distribute work between people. This makes more organized and using this way the 7 segment displays is a clever way to make a circuit more efficient.

Problems encountered:

Sometimes the frequeny divider didn’t work because VHDL versions but writing the code in different ways helped to make this project.